Claims:

1. A method for making a flat emitter comprising the steps of:

defining an emission region in a single crystal electron source;

forming at least a first epitaxial layer on said single crystal electron source; and

forming a thin conductor layer on said at least one epitaxial layer.

2. A method for making a flat emitter as defined by claim 1 wherein the steps of forming said at least a first epitaxial layer comprises forming said layer through atomic layer deposition.

3. A method for making a flat emitter as defined by claim 1 wherein the step of defining an emission region in said single crystal electron source comprises oxidizing a region proximate to said emission region.

4. A method for making a flat emitter as defined by claim 1 and further including the step of forming said single crystal electron source layer on an underlying single crystal electron source layer.

5. A method for making a flat emitter as defined by claim 1 wherein said at least a first epitaxial layer comprises a dielectric layer.

6. A method for making a flat emitter as defined by claim 1 wherein the step of forming said at least a first epitaxial layer comprises forming an epitaxial semi-conductor layer on said single crystal electron source and forming an epitaxial dielectric layer overlying said epitaxial semi-conductor layer.

7. A method for making a flat emitter as defined by claim 6 wherein said epitaxial dielectric layer is between about 1-5 nm thick, and wherein said epitaxial semiconductor layer is less than about 20 microns thick.

8. A method for making a flat emitter as defined by claim 1 wherein said thin conductor layer is an epitaxial conductor layer.

9. A method for making a flat emitter as defined by claim 8 wherein said epitaxial conductor layer is an N-doped semiconductor.

10. An electron emitter device comprising:
a single crystal electron source including an emission region;
a thin conductor layer; and
an epitaxial dielectric layer between said single crystal electron source and said thin conductor layer.

11. An emitter device as defined by claim 10 wherein said emitter is operative to emit electrons substantially free from electric field induced divergence.

12. An emitter device as defined by claim 10 wherein electrons are emitted from said thin conductor layer at a divergence of less than about 10° from perpendicular.

13. An emitter device as defined by claim 10 wherein said thin conductor layer is epitaxial.

14. An emitter device as defined by claim 10 wherein the emitter is operative to generate an electric field across said epitaxial dielectric layer to cause electrons to be emitted from said electron source emission region, to transport through said epitaxial dielectric layer, and to be emitted from said epitaxial conductor layer substantially free from electrical field induced divergence.

15. An emitter device as defined by claim 10 wherein said epitaxial dielectric layer is configured to promote a substantially uniform and uni-directional electric field across its thickness.

16. An emitter device as defined by claim 10 wherein said single crystal electron source comprises an epitaxial layer formed on a single crystal support.

17. An emitter device as defined by claim 16 wherein said emission region extends through the thickness of said epitaxial electron source layer to contact said single crystal support.

18. An emitter device as defined by claim 10 wherein said emission region has a perimeter substantially surrounded by a dielectric.

19. An emitter device as defined by claim 10 wherein the device is at least about 6% efficient.

20. An emitter device as defined by claim 10 wherein the device is at least about 10% efficient.

21. An emitter device as defined by claim 10 wherein said conductor layer has a substantially flat surface defining an emission surface of the emitter

22. An emitter device as defined by claim 10 wherein said epitaxial dielectric layer has a thickness of less than about 20 nm.

23. An emitter device as defined by claim 10 wherein said epitaxial dielectric layer has a thickness between about 2 and about 10 nm.

24. An emitter device as defined by claim 10 wherein said epitaxial dielectric layer is made of one of aluminum nitride or an oxide of silicon, aluminum, tantalum, titanium, hafnium, or zirconium.

25. An emitter device as defined by claim 10 and further including an epitaxial semi-conductor layer sandwiched between said electron source and said epitaxial dielectric layer.

26. An emitter device as defined by claim 28 wherein said epitaxial semi-conductor layer is less than about 20 microns thick.

27. An emitter device as defined by claim 26 wherein said epitaxial semi-conductor layer is between about 1 and about 5 microns thick.

28. An emitter device as defined by claim 10 wherein said conductor layer is less than about 7 nm thick.

29. An emitter device as defined by claim 10 and further including an electrical connection between said single crystal electron source and said thin epitaxial conductor layer, said connection linked to a potential sufficient to induce an electric field between said conductor layer and said electron source layer to cause electrons to be emitted from said electron source, to transport through said epitaxial layer, and to be emitted from said conductor layer substantially free from electrical field related divergence.

30. An emitter device as defined by claim 10 and further including a target, said conducting layer configured to direct said emitted electrons towards said target and to cause an effect on said target upon impact.

31. An emitter device as defined by claim 30 and further including focusing means positioned between said target and the emitter.

32. An emitter device as defined by claim 31 wherein said focusing means comprises an electrostatic focusing lens having an aperture in a conductor set at a predetermined voltage, said voltage adjustable to change the focusing effect of said focusing lens.

33. An emitter device as defined by claim 30 wherein said target comprises a memory, and wherein said effect comprises a physical change to said target, said physical change detectable through measurement of electrical properties of said memory.

34. An emitter device as defined by claim 33 wherein said emitter is operable to achieve a density of said physical changes of about a terabit per in^2 on said memory.

35. An emitter device as defined by claim 30 wherein said target comprises a display having a plurality of pixels, and wherein said effect comprises a visual change in one of said pixels when said emitted electrons are received by said one of said pixels.

36. An emitter device as defined by claim 30 and further including a mover connected to one or more of the emitter or said target for moving said one or more of the emitter or said target.

37. An integrated circuit including a plurality of the emitter devices as defined by claim 10 and further including control circuitry connected to said plurality of emitter devices.

38. An emitter memory device including a plurality of the emitter devices as defined by claim 10 arranged in an array, further including a memory, and further including a plurality of focusing lens arranged to cooperate with said array of emitter devices, each of said focusing lens configured to focus electrons emitted from one of said emitter devices and to direct said focused

electrons towards said memory, said focused electrons causing a structural phase change in said memory upon impact, said structural phase changes having a density of about a terabit per in^2 on said memory, and an integrated reader circuit for detecting said structural phase change through measurement of electrical properties.

39. A method for emitting electrons from an emitter comprising the steps of:

generating an electric field across an epitaxial dielectric layer from a thin conductor layer, said electric field substantially uniform and free from geometrical based divergence, said electric field operative to cause electrons to be emitted from said electron source, to transport through said epitaxial dielectric layer, and to be emitted from said thin dielectric conductor layer.

40. A method for emitting electrons as defined by claim 39 and further including the step of causing said electrons to transport through an epitaxial semi-conductor layer positioned between said electron source and said epitaxial dielectric layer.

41. A method for emitting electrons as defined by claim 39 wherein said electrons are emitted at an angle of less than about 10° from perpendicular from said conductor layer.

42. A method for emitting electrons as defined by claim 39 wherein the method further includes the step of directing said emitted electrons at an anode target, and of causing an effect in said target when said emitted electrons strike said target, said target comprising one of a memory or a display, and said effect being detectable through measurement of an electrical property.

43. A method for emitting electrons as defined by claim 39 wherein said electrons are emitted at an efficiency of at least about 6%.